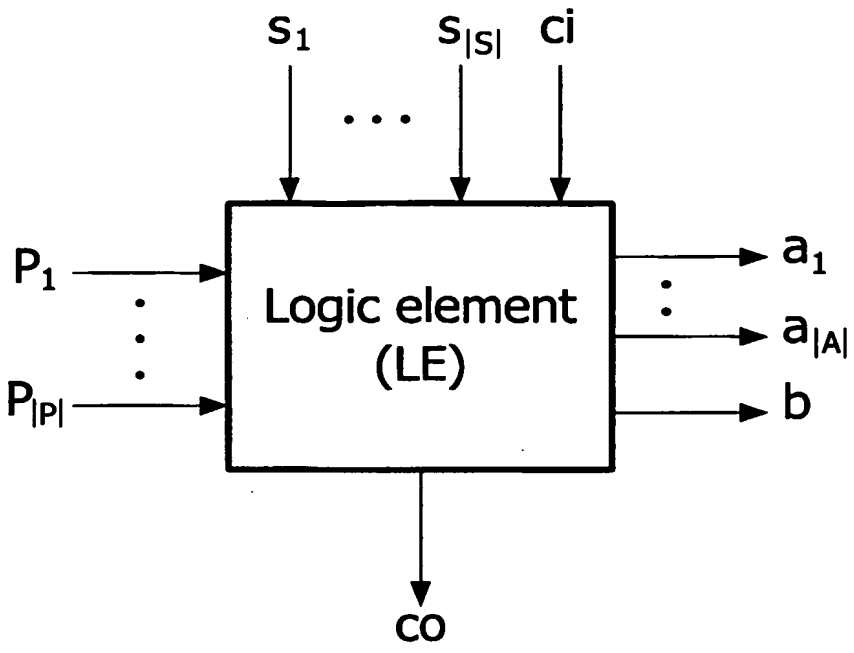

FIG. 1

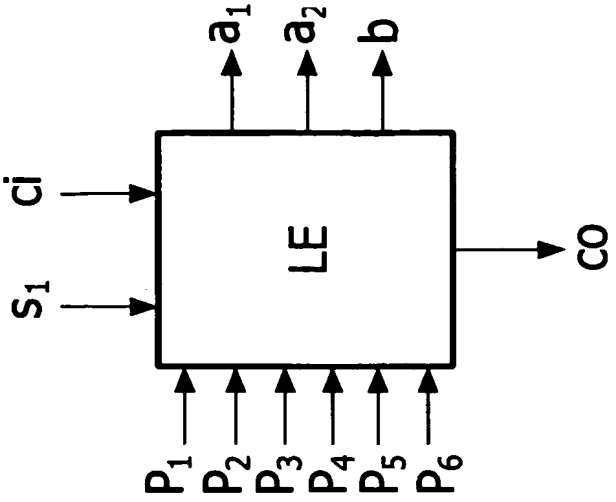

FIG. 2c

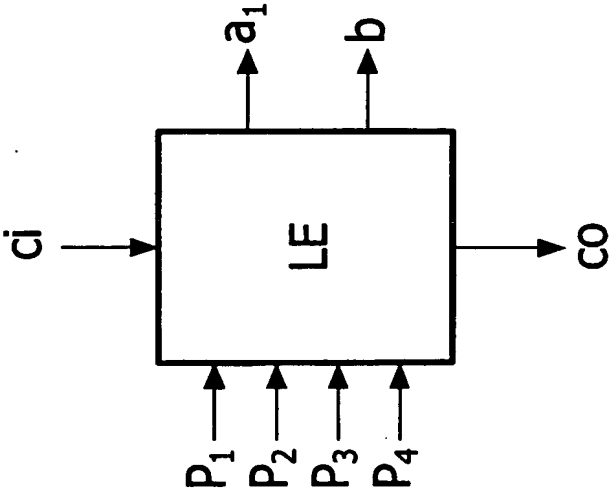

FIG. 2b

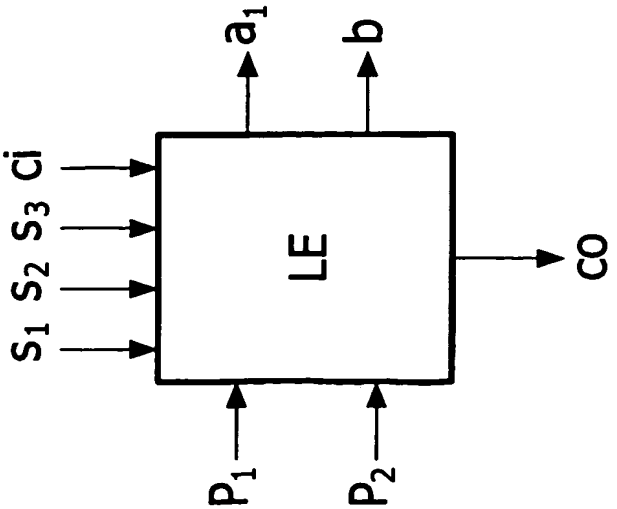

FIG. 2a

TYPE	|P|	|S|	|A|
Data-path oriented	2	3	1
Random-logic oriented	4	0	1
Memory-oriented	6	1	2

FIG. 3

TYPE	Boolean	Arithmetic	Memory
Data-path oriented	2	1	-
Random-logic oriented	4	1	-
Memory-oriented	5	2	2

FIG. 4

TYPE	|X|	|S|	|Y|
Data-path oriented	2*|N|	3	|N|
Random-logic oriented	max(log|N| + 4,2*|N|)	0	|N|
Memory-oriented	6*|N|	1	2*|N|

FIG. 6

TYPE	Boolean	Arithmetic	Memory
Data-path oriented	log|N| + 2	|N|	-
Random-logic oriented	log|N| + 4	|N|	-
Memory-oriented	log|N| + 5	2*|N|	2*|N|

FIG. 7

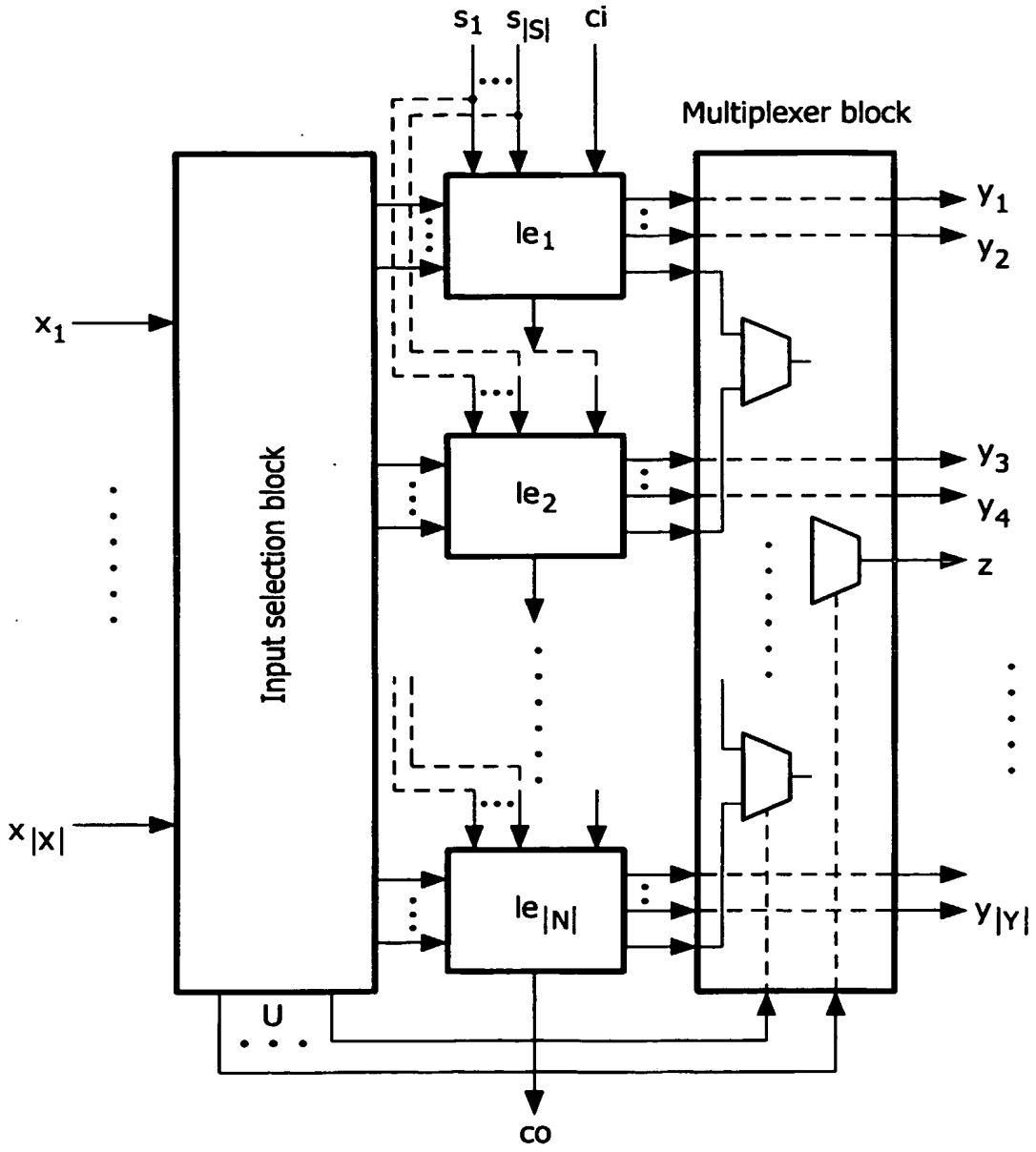
s1
s|S|
ci
Multiplexer block
le1
le2
le|N|
Input selection block
x1
x|X|
y1
y2
y3
y4
z
y|Y|
U
co

FIG. 5

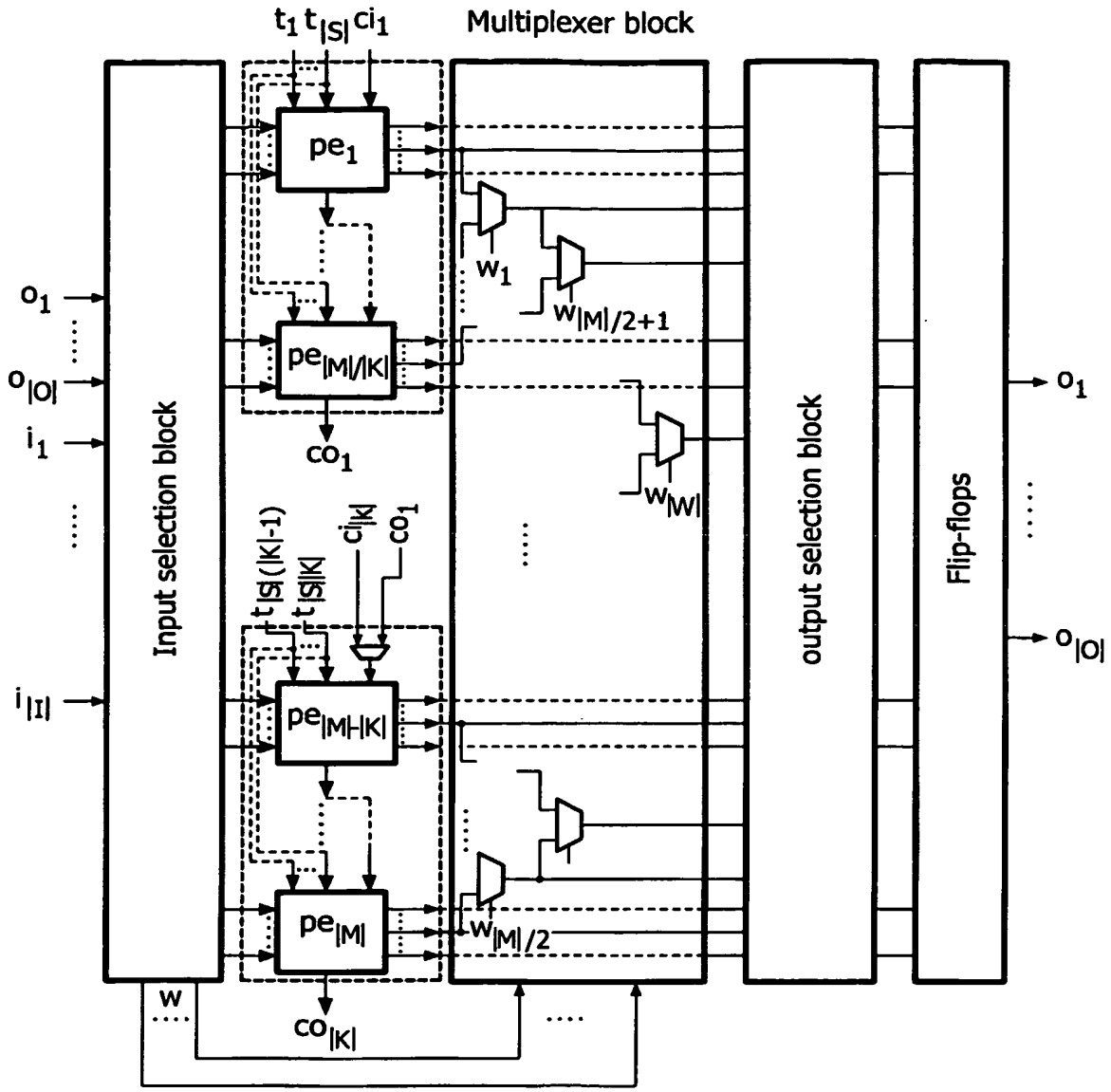
t1 t|S| ci1
Multiplexer block
pe1
pe|M|/|K|
co1
pe|M|-|K|
pe|M|
co|K|
w1
w|M|/2+1
w|M|
w|M|/2
o1
o|O|
i1
i|I|
Input selection block
output selection block
Flip-flops
t|S|(|K|-1)
t|S|K
ci|K|
co1
w

FIG. 8

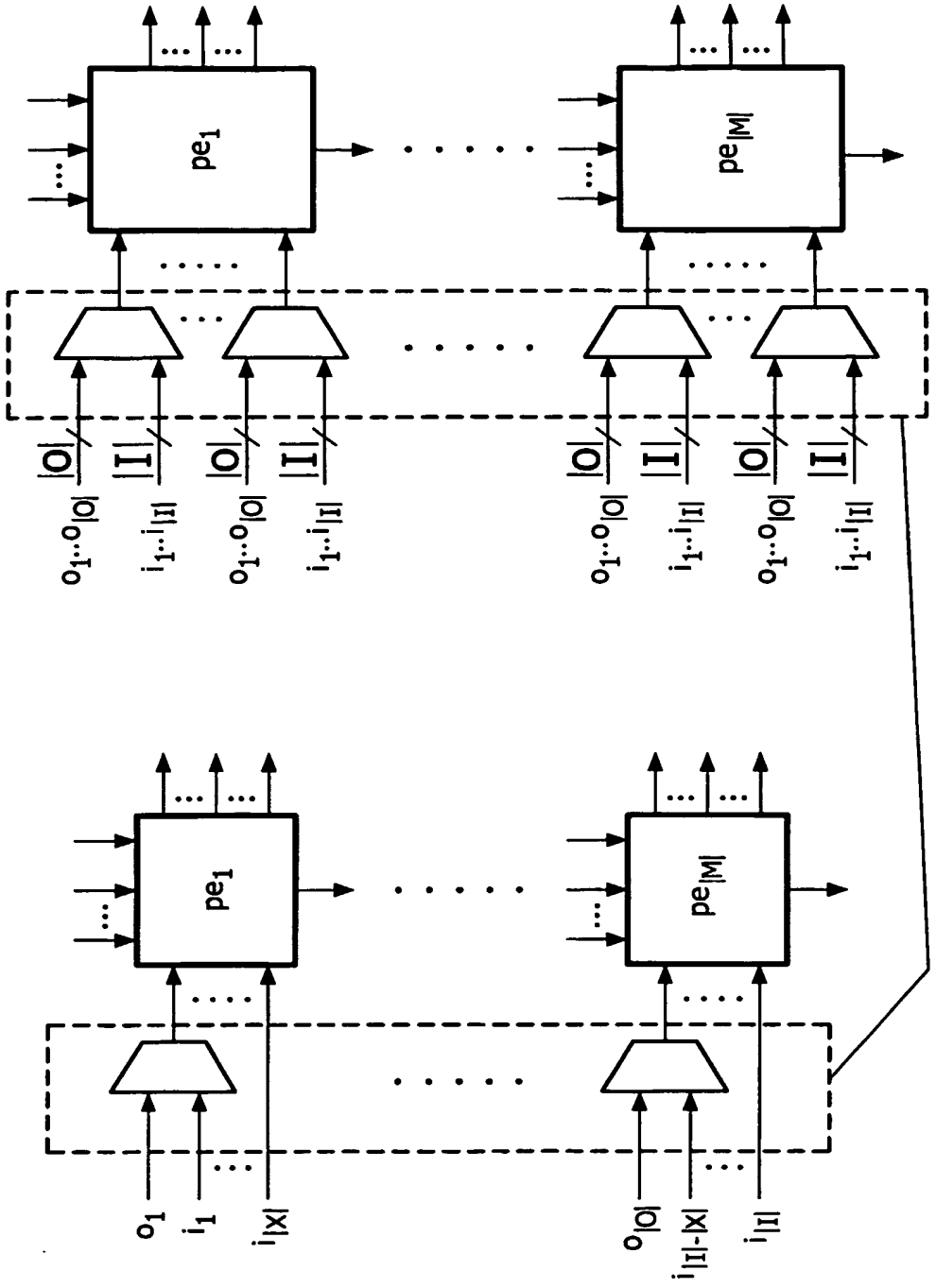

FIG. 9b

FIG. 9a

TYPE	I	O
Data-path oriented	|X|*|M|	|Y|*|M|
Random-logic oriented	max(|X|/2*(|M| +1), |X|*|M|*2)	|Y|*|M|
Memory-oriented	|X|*|M|	|Y|*|M|

FIG. 10

TYPE	Boolean	Arithmetic	Memory
Data-path oriented	log|M|* (log|N| + 2)	|M|*|N|	-
Random-logic oriented	log|M|* (log|N| + 4)	|M|*|N|	-
Memory-oriented	log|M|* (log|N| + 5)	2*|M|*|N|	2*|M|*|N|

FIG. 11

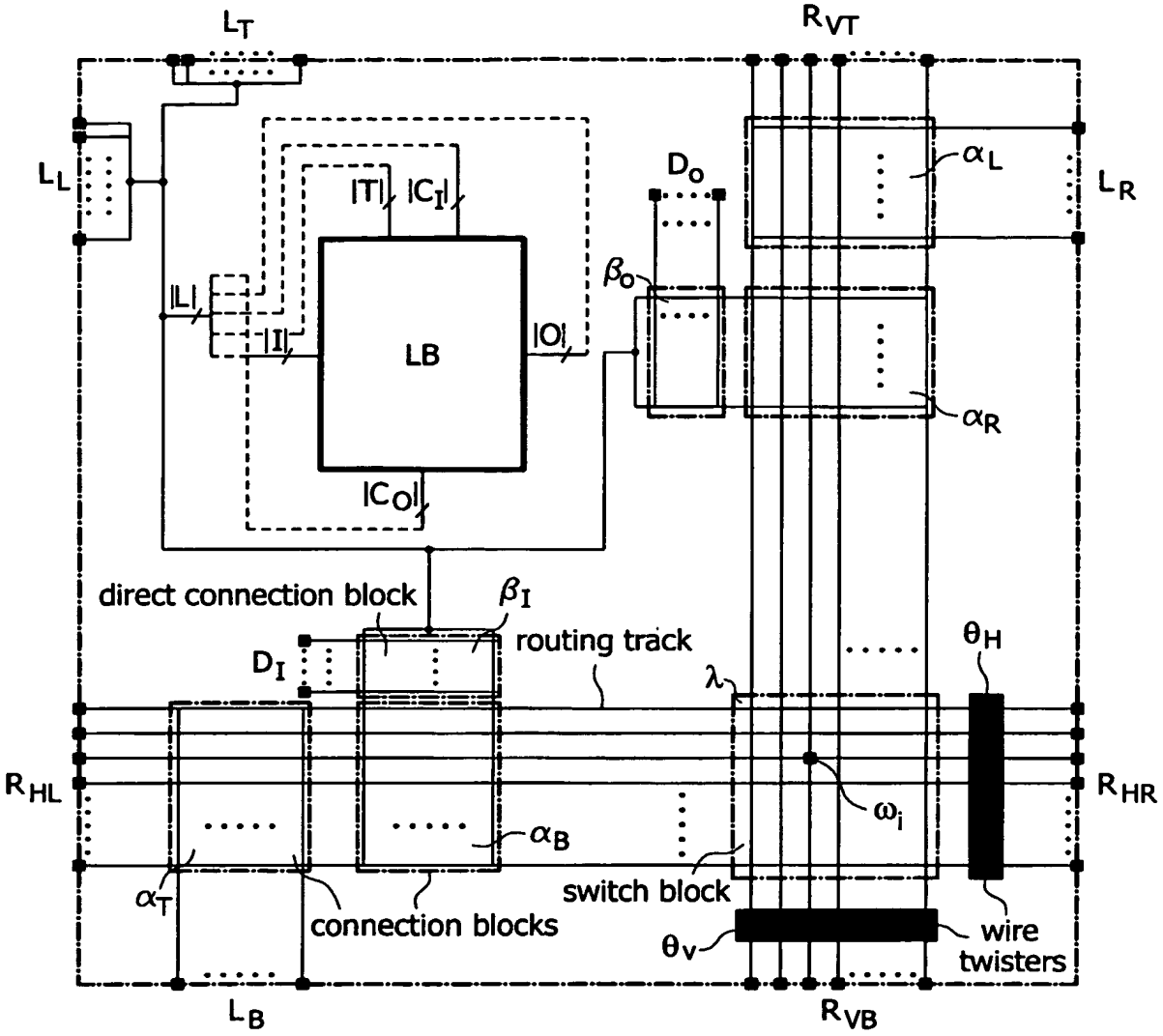
L_T
R_{VT}
L_L
L_R
D_O
α_L
β_O
|T|
$|C_I|$
|L|
|I|
LB
|O|
α_R
$|C_O|$
direct connection block
β_I
routing track
θ_H
D_I
λ
R_{HL}
R_{HR}
ω_i
α_B
α_T
switch block
connection blocks
θ_V
wire twisters
L_B
R_{VB}

FIG. 12

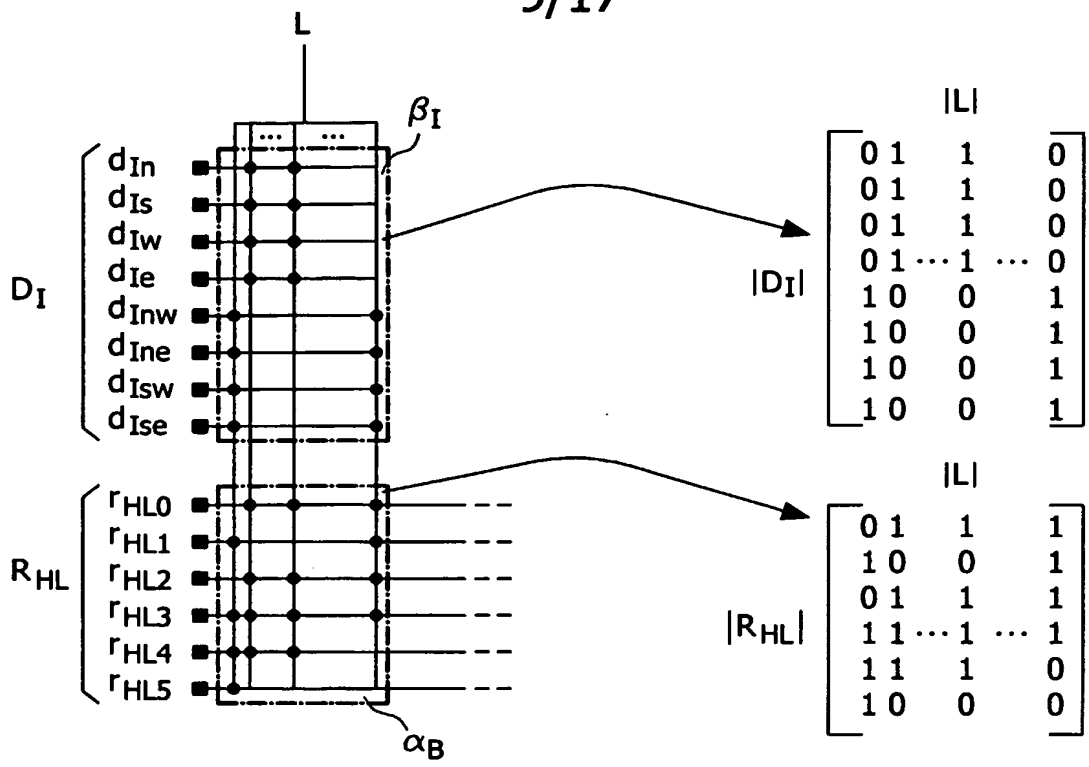

FIG. 13a

FIG. 13b

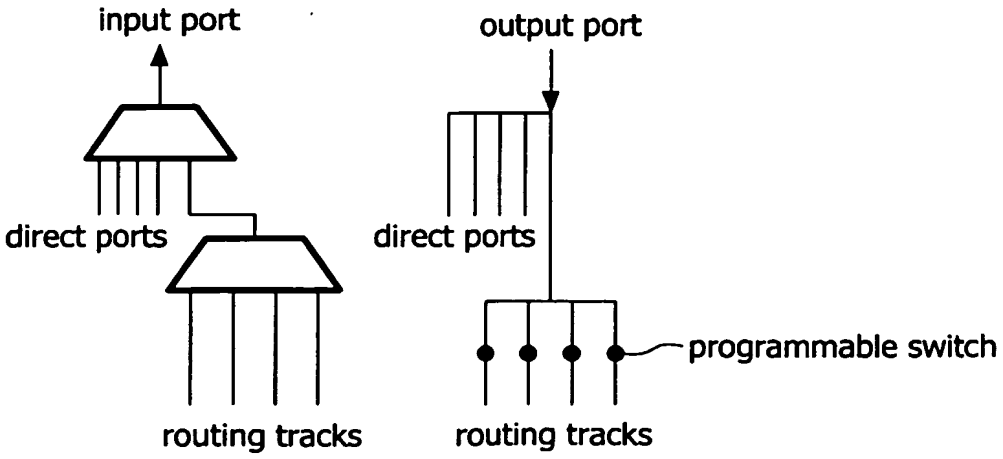

FIG. 13c

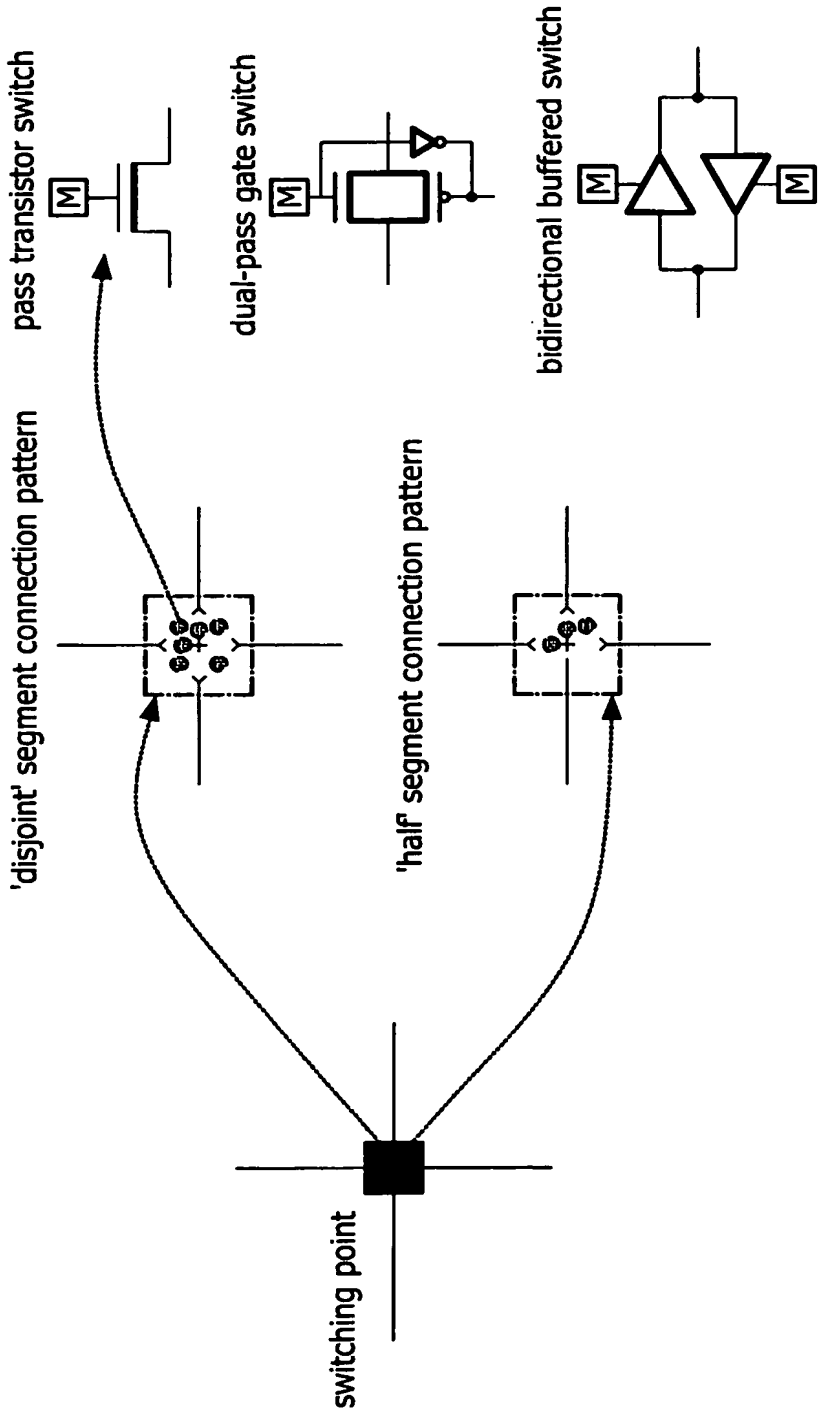

FIG. 14b

FIG. 14a

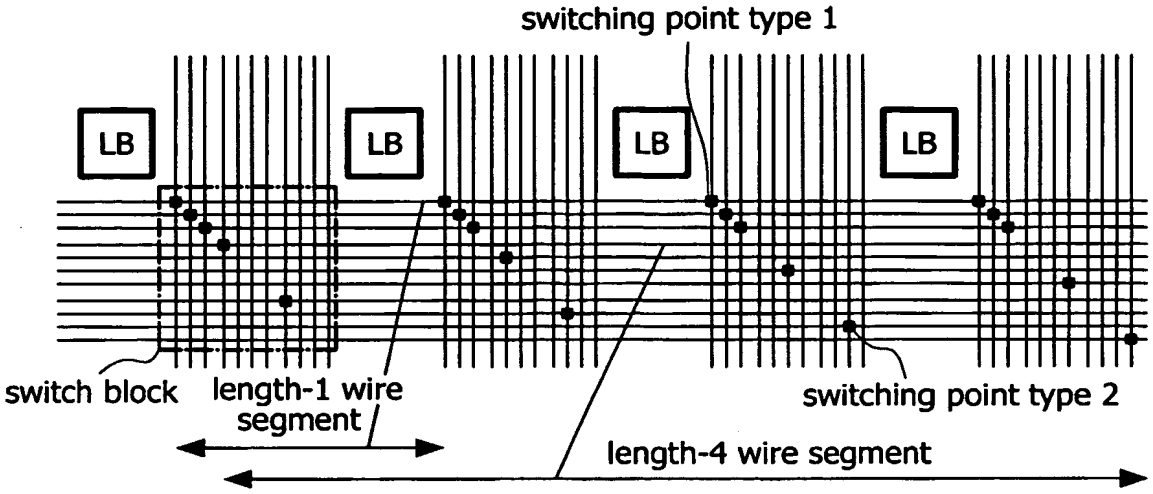

FIG. 15a

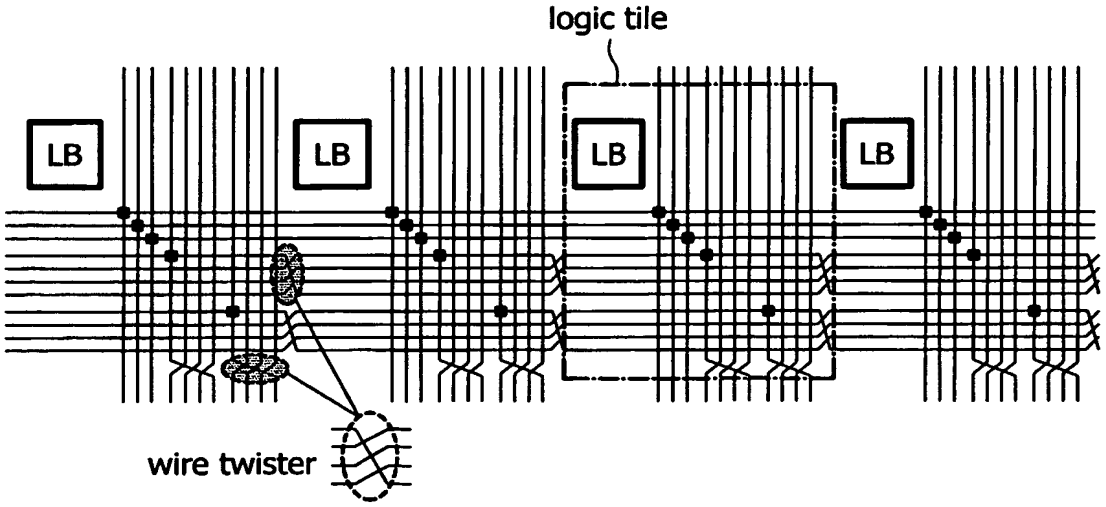

FIG. 15b

Switching matrix

$$\begin{bmatrix} 1&0&0&0&0&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0&0&0&0&0 \\ 0&0&0&2&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&2&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&0 \end{bmatrix}$$

Twist matrix

$$\begin{bmatrix} 1&0&0&0&0&0&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0&0&0&0&0&0 \\ 0&0&1&0&0&0&0&0&0&0&0&0 \\ 0&0&0&0&0&0&1&0&0&0&0&0 \\ 0&0&0&1&0&0&0&0&0&0&0&0 \\ 0&0&0&0&1&0&0&0&0&0&0&0 \\ 0&0&0&0&0&1&0&0&0&0&0&0 \\ 0&0&0&0&0&0&0&0&0&0&0&1 \\ 0&0&0&0&0&0&0&1&0&0&0&0 \\ 0&0&0&0&0&0&0&0&1&0&0&0 \\ 0&0&0&0&0&0&0&0&0&1&0&0 \end{bmatrix}$$

FIG. 15c

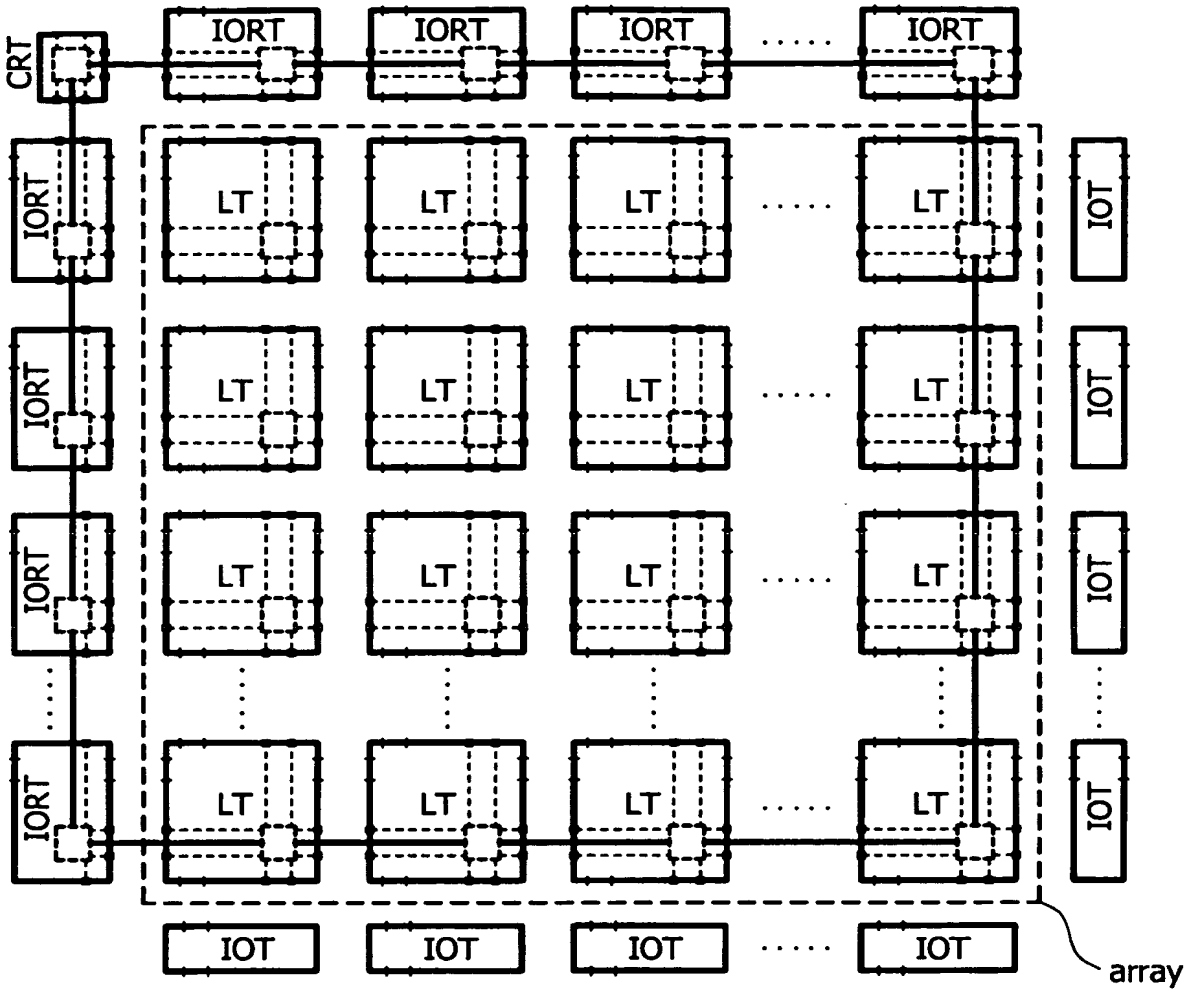
CRT
IORT
IORT
IORT
IORT
IORT
IORT
IORT
IORT
LT
IOT
IOT
IOT
IOT
IOT
IOT
IOT
IOT
array

FIG. 16

Input/Output Tile with Routing (IORT): top

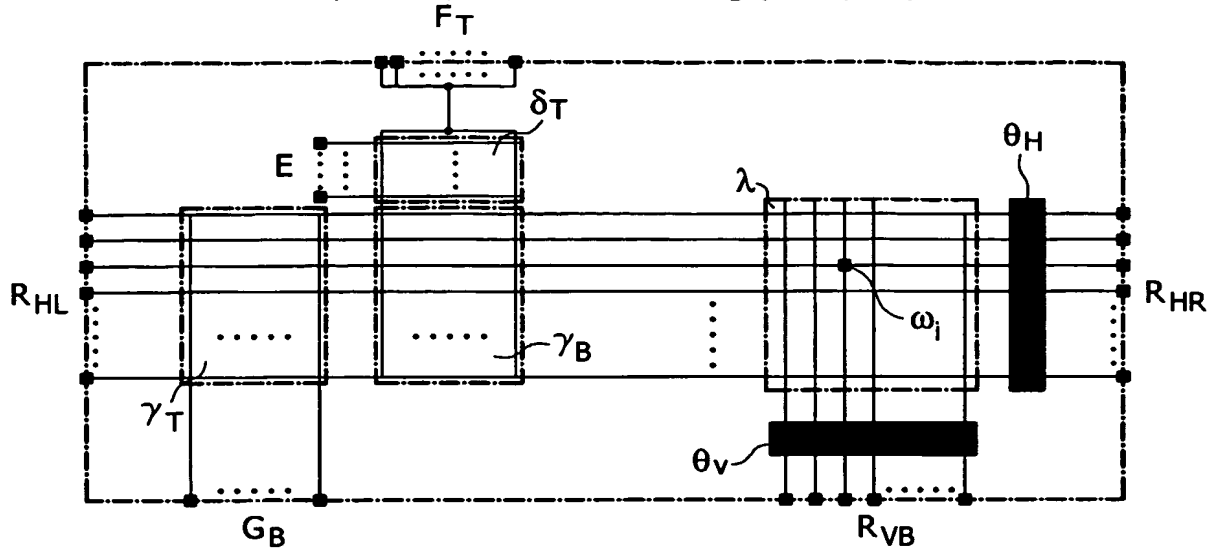

FIG. 17a

Input/Output Tile with Routing (IORT): left

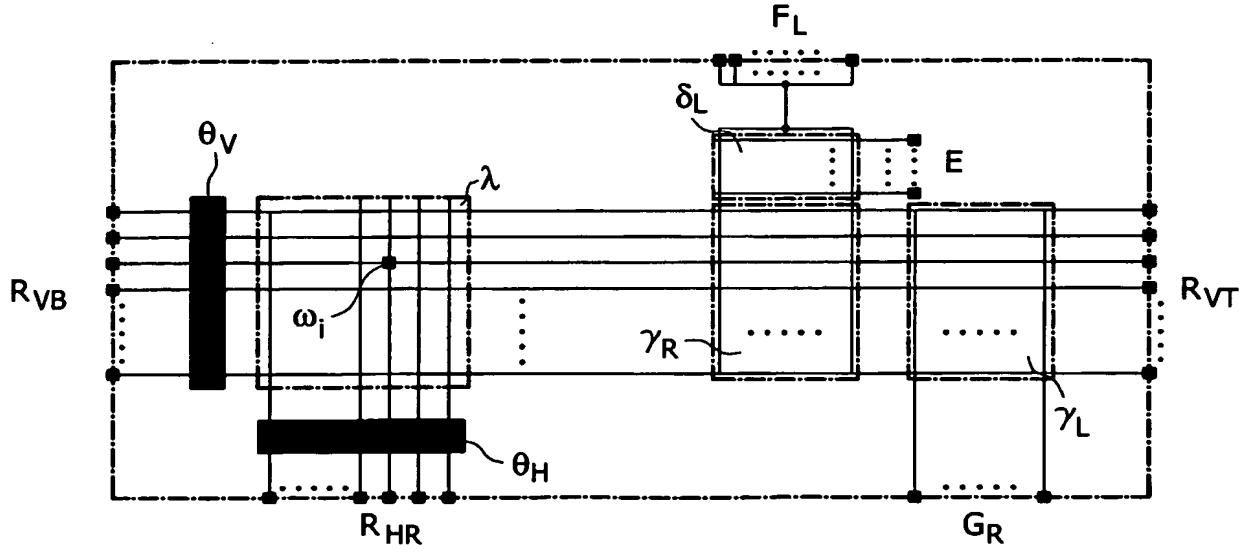

FIG. 17b

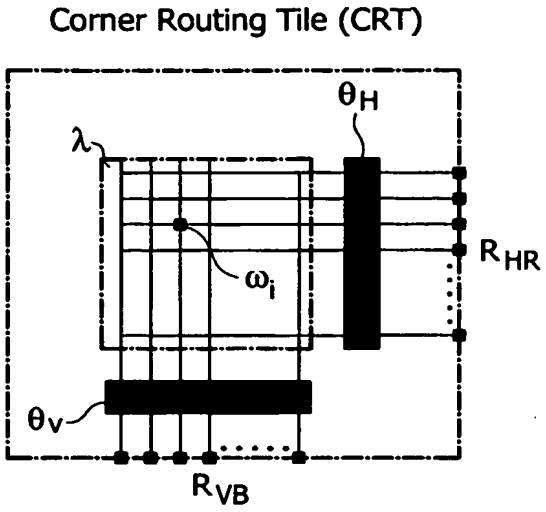

FIG. 17c

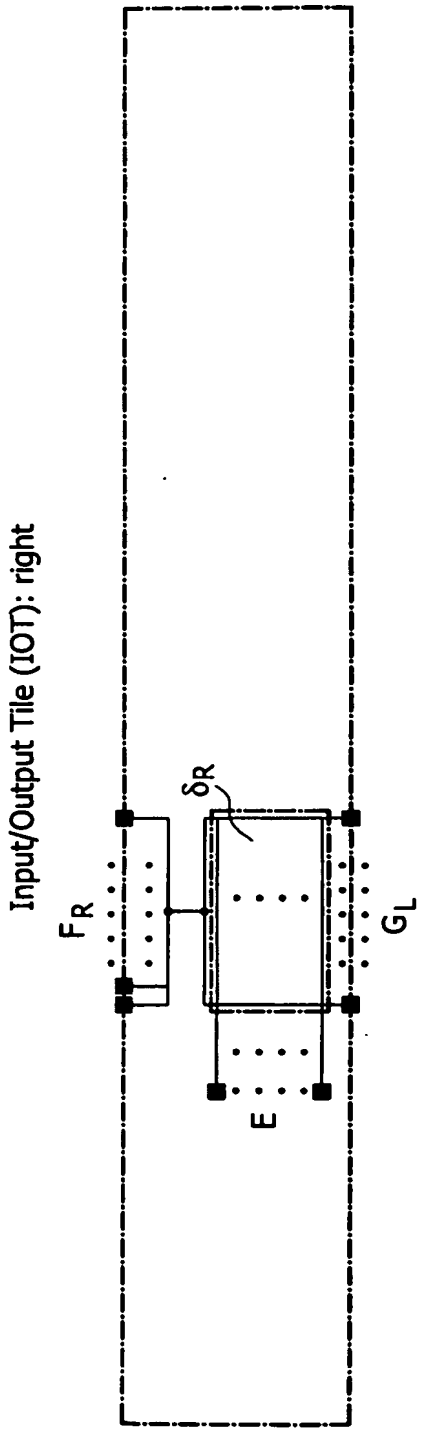

FIG. 18a

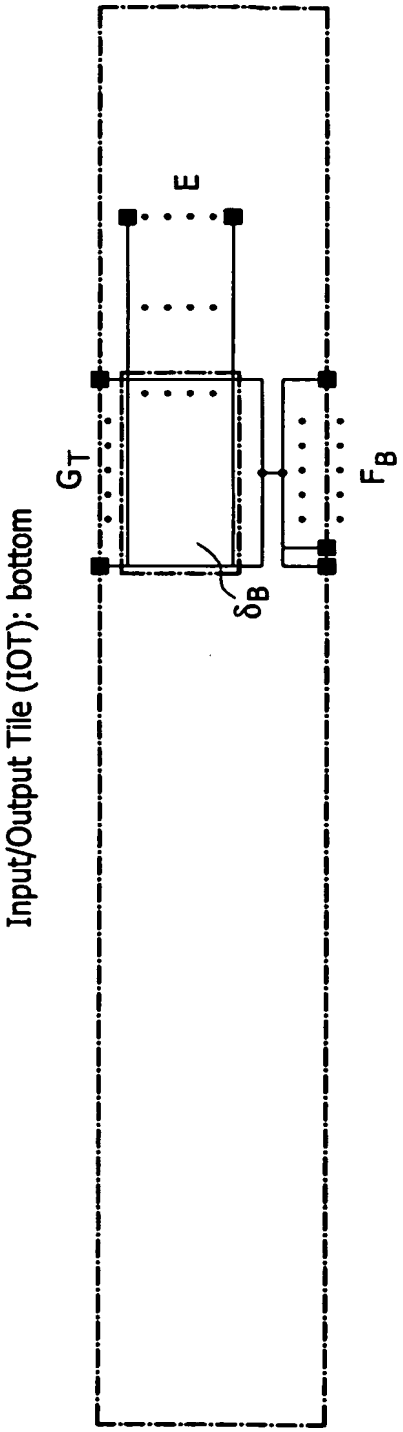

FIG. 18b

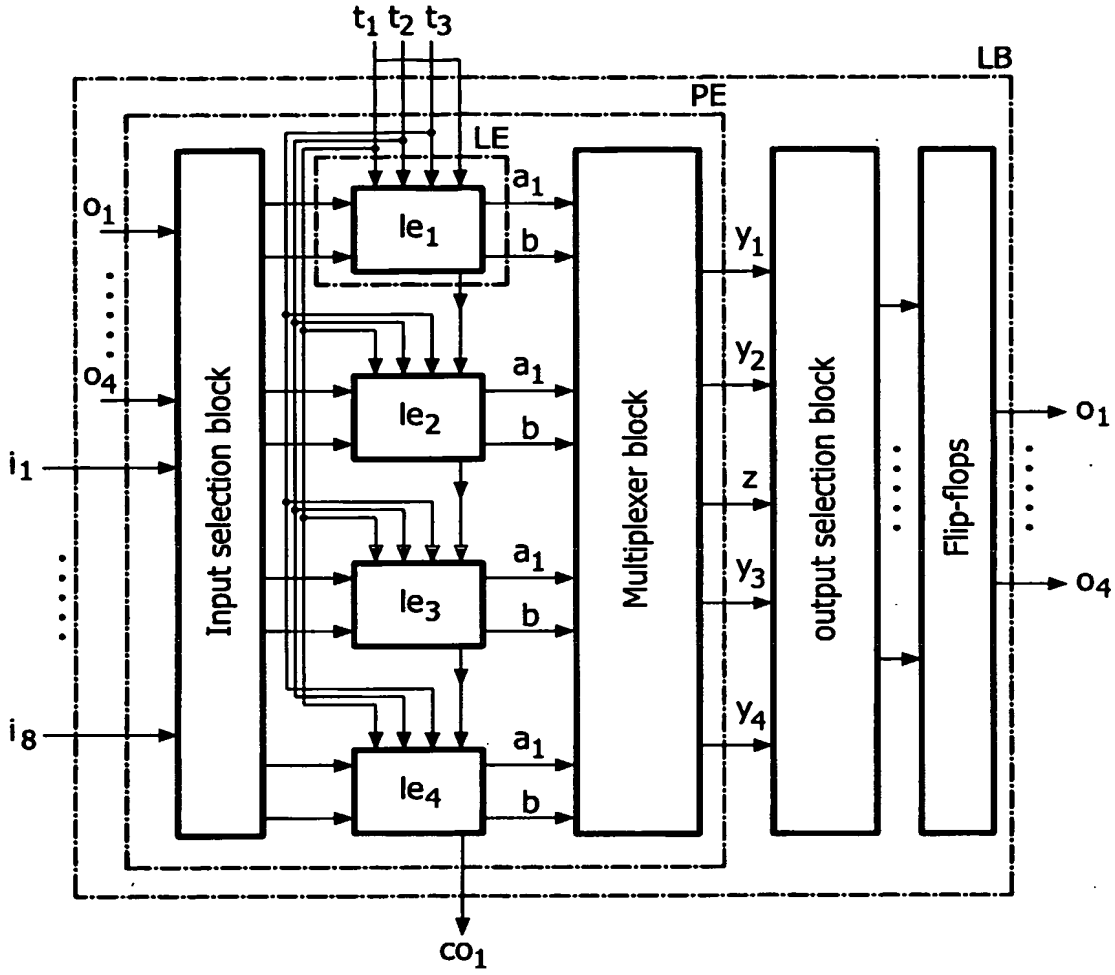
t1 t2 t3
LB
PE
LE
o1
o4
i1
i8
Input selection block
le1
le2
le3
le4
a1
b
Multiplexer block
y1
y2
z
y3
y4
output selection block
Flip-flops
o1
o4
co1

FIG. 19